A GEOMETRIC D/A CONVERTER FOR A DELAY-LOCKED LOOP

Related Applications

This is a continuation of Application Serial No. 10/396,884 filed March 25, 2003, which is now a U.S Patent 6,734,815. This application is incorporated herein by reference.

Background of the Invention

1. Field of the Invention

This invention relates generally to digital-to-analog converters (DACs), and more particularly to a geometric D/A converter architecture that can be used to implement a delay-locked loop (DLL) with a digital control loop.

2. Description of the Prior Art

The general architecture of a DLL 100 with a digital control loop is shown in Figure 1. The DLL 100 includes of a delay line 102 with controllable delay (shown as a chain of buffers in the Figure). The control signal 104 is analog. DLL 100 further includes a phase detector 106 (shown as pd) which compares the input and output clock signals 108, 110 of the delay line 102 and issues an appropriate signal in response to a mismatch. The DLL 100 also includes a filter and state machine 112 which receives the phase detector results and makes an appropriate decision with regard to any delay increase or decrease. Finally, DLL 100 can also be seen to include a D/A converter 120 (shown and referred to herein after as DAC), which converts the filter and state machine 112 results from digital format to analog, which are then fed to the delay line control line 104.

The cells of delay line 102 can be, for example, current starved inverters, meaning that the delay of each cell is controlled by varying the amount of current available for switching. In this implementation, the output of the DAC 120 is a current. The delay of a current starved inverter is known to be proportional to C·Vdd/I, where C is the input capacitance of the gate, Vdd is the supply voltage, and I is the current supplied to the cell.